Design of Digital Systems II

Combinational Logic Design Practices (1)

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Circuit Timing

- Outputs of real circuits take time to react to their inputs
- Most digital systems are sequential circuits
  - Operate step-by-step under control of a periodic clock signal
  - Speed of clock is limited by the worst-case time that it takes for operations in one step to complete
- The greatest challenge in completing a board-level or an ASIC design is achieving required timing performance

Circuit Timing: Timing Diagrams

- **Timing diagram**
  - Illustrates logical behavior of signals in a digital circuit as a function of time
  - Arrows are drawn to show causality
    - Which input transitions cause which output transitions
  - The most important information is a specification of delay between transitions
    - Different paths through a circuit may have different delays
    - Delay through any given path may vary depending on whether output is changing from LOW to HIGH or from HIGH to LOW
  - Since delays can vary depending on voltage, temperature, and manufacturing parameters, delay is seldom specified as a single parameter
    - Minimum, typical, and maximum values

Circuit Timing: Timing Diagrams

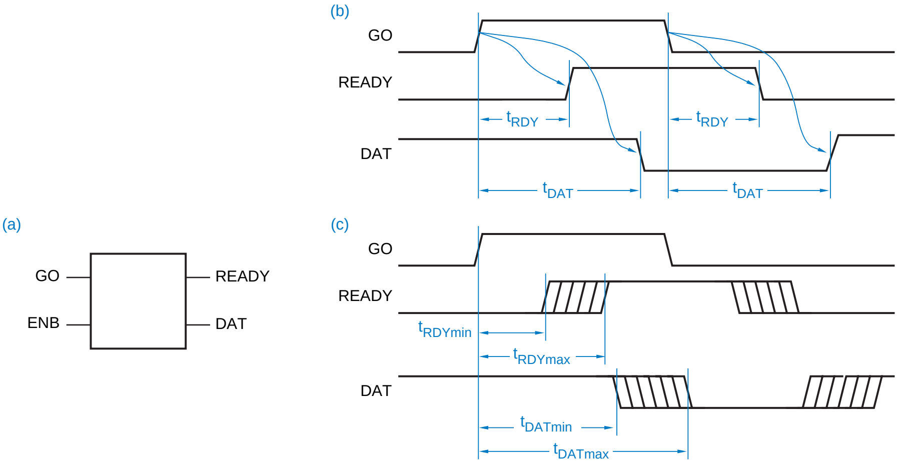

Figure 1: Timing diagrams for a combinational circuit: (a) block diagram of circuit; (b) causality and propagation delay; (c) minimum and maximum delays.

Circuit Timing: Timing Diagrams

- For any signal that carries a bit of data, timing diagram needn't show whether signal changes from 1 to 0 or from 0 to 1 at a particular time, only that a transition occurs then
- A group of data signals in a bus is often processed by identical circuits
  - Hence, all signals in bus have same timing, and can be represented by a single line in timing diagram

Circuit Timing: Timing Diagrams

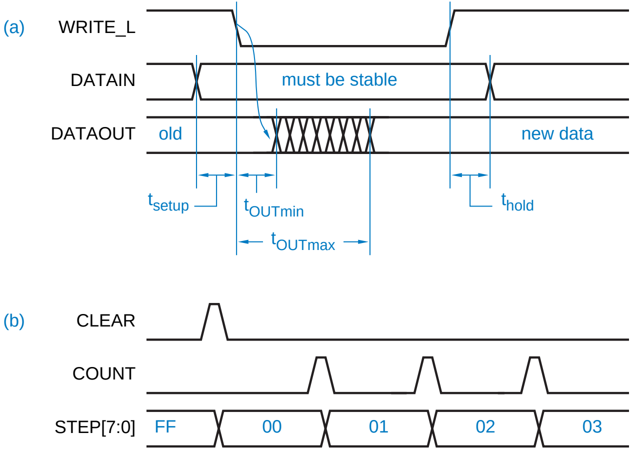

Figure 2: Timing diagrams for data signals: (a) certain and uncertain transitions; (b) sequence of values on an 8-bit bus.

Circuit Timing: Propagation Delay

- Propagation delay of a signal path is time that it takes for a change at input of path to produce a change at output of path
- A combinational circuit with many inputs and outputs has many different paths
  - Each one may have a different propagation delay
- Propagation delay when output changes from LOW to HIGH (t_{pLH}) may be different from delay when it changes from HIGH to LOW (t_{pHL})

Combinational Programmable Logic Devices (PLDs)

- There are a large variety of ICs that can have their logic function "programmed" into them after they are manufactured
- Most of these devices use technology that also allows function to be reprogrammed
    - If you find a bug in your design, you may be able to fix it without physically replacing or rewiring device

Combinational PLDs: Programmable Logic Arrays (PLAs)

- Historically, first PLDs were PLAs
- A PLA is a combinational, two-level AND-OR device that can be programmed to realize any sum-of-products logic expression, subject to size limitations of device
- Limitations are
  - Number of inputs (n)
  - Number of outputs (m)
  - Number of product terms (p)
- In general, p is far less than number of n-variable minterms (2^n)
  - Thus, a PLA cannot perform arbitrary n-input, m-output logic functions
  - Its usefulness is limited to functions that can be expressed in SOP form using p or fewer product terms
- An $n \times m$ PLA with p product terms contains p $2n$-input AND gates and m p-input OR gates

Combinational PLDs: Programmable Logic Arrays (PLAs)

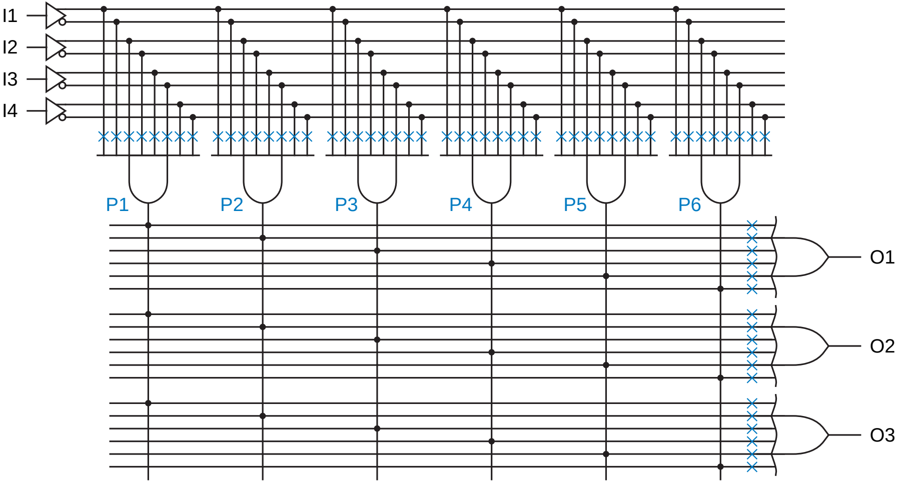

Figure 3: A 4 × 3 PLA with six product terms.

Combinational PLDs: Programmable Logic Arrays (PLAs)

- Each input connects to a buffer/inverter that produces both a true and a complemented version of signal for use within array
- Potential connections in array are indicated by X's
  - Device is programmed by keeping only connections that are actually needed
  - Selected connections are made by **fuses**, which are not actually fuses, but nonvolatile memory cells that can be programmed to make a connection or not

Combinational PLDs: Programmable Logic Arrays (PLAs)

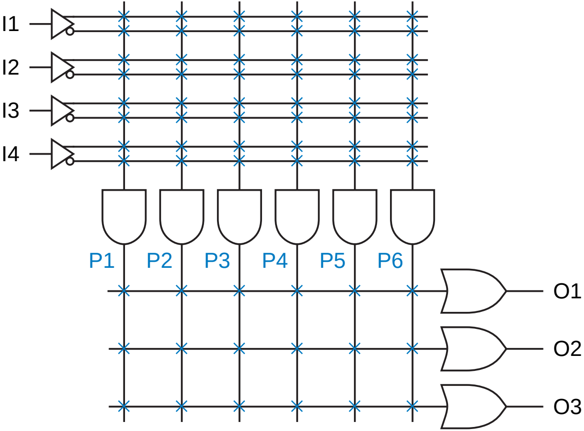

Figure 4: Compact representation of a 4 × 3 PLA with six product terms.

Combinational PLDs: Programmable Logic Arrays (PLAs)

- PLA in Fig. 4 can perform any three 4-input combinational logic functions that can be written as SOPs using a total of six or fewer distinct product terms, e.g.

$$O1 = I1 \cdot I2 + I1' \cdot I2' \cdot I3' \cdot I4'$$
$$O2 = I1 \cdot I3' + I1' \cdot I3 \cdot I4 + I2$$
$$O3 = I1 \cdot I2 + I1 \cdot I3' + I1' \cdot I2' \cdot I4'$$

  - These equations have a total of eight product terms, but first two terms in $O3$ are same as first terms in $O1$ and $O2$
  - Programmed connection pattern in Fig. 5 matches these logic equations

Combinational PLDs: Programmable Logic Arrays (PLAs)

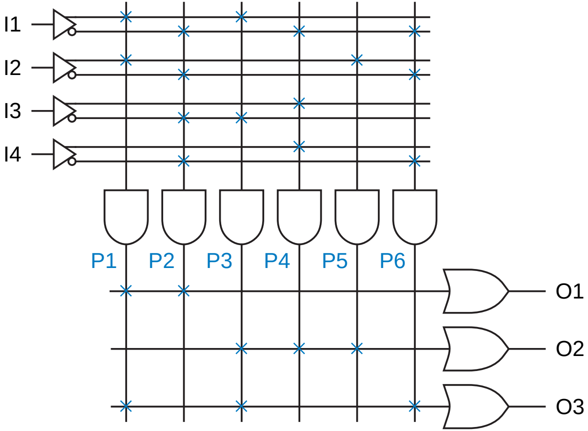

Figure 5: A 4 × 3 PLA programmed with a set of three logic equations.

Combinational PLDs: Programmable Logic Arrays (PLAs)

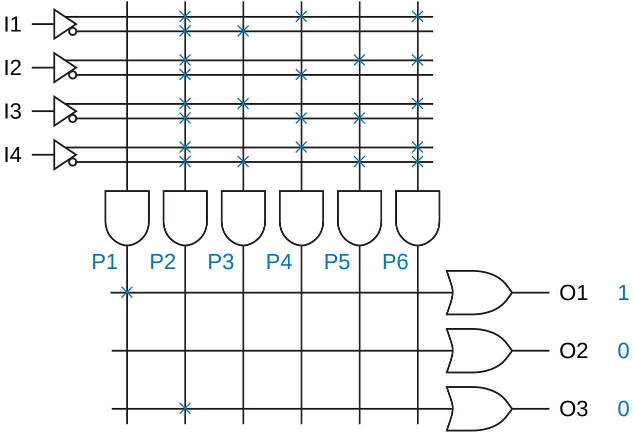

Figure 6: A 4 × 3 PLA programmed to produce constant 0 and 1 outputs.

Combinational PLDs: Programmable Array Logic (PAL)

- A special case of a PLA, and basis of today's most commonly used PLDs, is PAL device
- Unlike a PLA, a PAL device has a fixed OR array
- PAL devices also use bidirectional input/output pins
- One of today's most commonly used combinational PLD structures is "PAL16L8"

Combinational PLDs: Programmable Array Logic (PAL)

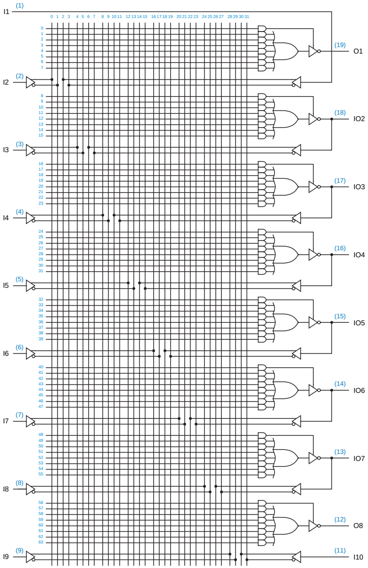

Figure 7: Logic diagram of the PAL16L8.

Combinational PLDs: Programmable Array Logic (PAL)

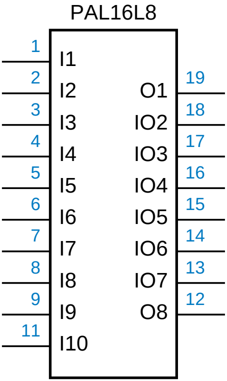

Figure 8: Logic symbol for the PAL16L8.

Combinational PLDs: Programmable Array Logic (PAL)

- PAL16L8
  - Its programmable AND array has 64 rows and 32 columns and $64 \times 32 = 2048$ fuses
  - Each of 64 AND gates in array has 32 inputs, accommodating 16 variables and their complements
  - Eight AND gates are associated with each output pin
    - Seven of them provide inputs to a fixed 7-input OR gate
    - The eighth (called *output-enable gate*) is connected to three-state enable input of output buffer
  - Buffer is enabled only when output-enable gate has a 1 output
  - An output can perform only logic functions that can be written as sums of seven or fewer product terms
    - Each product term can be a function of any or all 16 inputs
  - Although PAL16L8 has up to 16 inputs and up to 8 outputs, it is housed in a dual in-line package with only 20 pins, including two for power and ground (pins 10 and 20)
    - This is result of six bidirectional pins (13–18) that may be used as inputs or outputs or both

Combinational PLDs: Programmable Array Logic (PAL)

- PAL16L8
  - Six of output pins, called *I/O pins*, may also be used as inputs
  - If an I/O pin's output-control gate produces a constant 0, then output is always disabled and pin is used strictly as an input
  - If input signal on an I/O pin is not used by any gates in AND array, then pin may be used strictly as an output
    - Depending on programming of output-enable gate, output may always be enabled, or it may be enabled only for certain input conditions
  - If an I/O pin's output-control gate produces a constant 1, output is always enabled, but pin may still be used as an input too
    - In this way, outputs can be used to generate first-pass "helper terms" for logic functions that cannot be performed in a single pass with limited number of AND terms available for a single output
  - With an I/O pin always output-enabled, output may be used as an input to AND gates that affect the very same output
    - That is, we can embed a feedback sequential circuit

Combinational PLDs: Generic Array Logic Devices

- Sequential PLDs are programmable logic devices that provide flip-flops at some or all OR-gate outputs
- One type of sequential PLD is called generic array logic or a GAL device
- GAL16V8
  - Can be configured to emulate AND-OR, flip-flop, and output structure of any of a variety of combinational and sequential PAL devices
  - Can be erased and reprogrammed
    - Its fuses are nonvolatile memory cells
  - When configured as a combinational device (similar to PAL16L8) is called GAL16V8C

Combinational PLDs: Generic Array Logic Devices

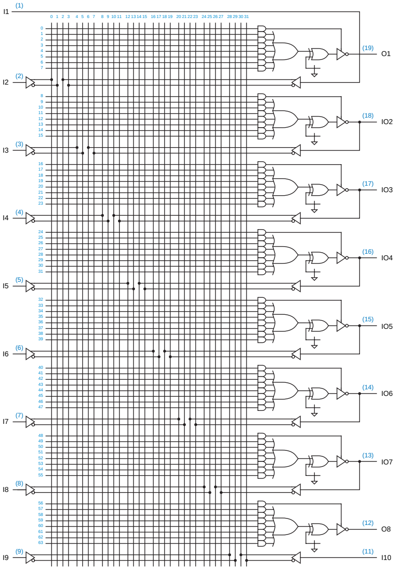

Figure 9: Logic diagram of the GAL16V8C.

Combinational PLDs: Generic Array Logic Devices

- GAL16V8C
  - An XOR gate is inserted between each OR output and three-state output driver
  - One input of XOR gate is pulled up to a logic 1 value but connected to ground via a fuse
    - If fuse is intact, XOR gate passes OR-gate's output unchanged
    - If fuse is blown, XOR gate inverts OR-gate's output
    - Fuse controls *output polarity* of corresponding output pin
  - Given a logic function to minimize, we find minimal SOP expressions for both function and its complement
    - If complement yields fewer product terms, it can be used if GAL16V8's output polarity fuse is set to invert

Combinational PLDs: CPLDs

- **Complex programmable logic device (CPLD)**
    - A collection of individual PLDs on a single chip, accompanied by a programmable interconnection and input/output structure
    - Individual PLDs have at least functionality of GAL devices
    - **CPLD fitter**
        - Starting with an HDL description of desired function, a synthesis tool *fits* the function into an available CPLD device, often the smallest possible
        - The synthesis tool is called a *fitter*
        - Fitter minimizes equation for each PLD output
        - It also partitions function into individual PLD blocks, and then tries to find the smallest possible device that has enough PLD blocks, product terms, internal connections, and external input/output pins
        - Fitters allow designer to specify *constraints*, such as "put these outputs together in the same PLD block"

Combinational PLDs: CPLDs

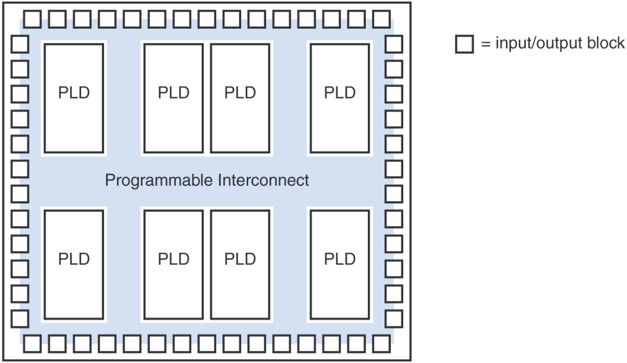

Figure 10: General CPLD architecture.

Combinational PLDs: Bipolar PLD Circuits

- Early PLA and PAL devices used bipolar circuits

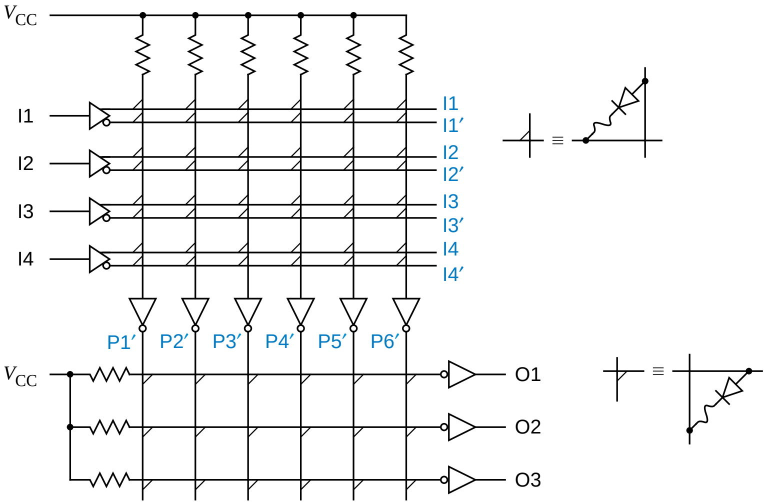

Figure 11: A 4 × 3 PLA built using TTL-like open-collector gates and diode logic.

Combinational PLDs: Bipolar PLD Circuits

- In Fig. 11
  - Each potential connection is made by a diode in series with a metal link
  - If link is present, diode connects its input into a diode-AND function
  - If link is missing, corresponding input has no effect on that AND function
  - A diode-AND function is performed because each horizontal input line that is connected via a diode to a particular vertical AND line must be HIGH in order for that AND line to be HIGH
  - If an input line is LOW, it pulls LOW all of AND lines to which it is connected
  - Each AND line is followed by an inverting buffer, so overall a NAND function is obtained
  - Outputs of first-level NAND functions are combined by another set of NAND functions
  - A two level NAND-NAND structure is equivalent to AND-OR structure
- A bipolar PLD chip is manufactured with all of its diodes present, but with a tiny fusible link in series with each one
  - By applying special input patterns to device, it is possible to select individual links, apply a high voltage and vaporize selected links

Combinational PLDs: CMOS PLD Circuits

- CMOS PLDs reduce power consumption and are reprogrammable

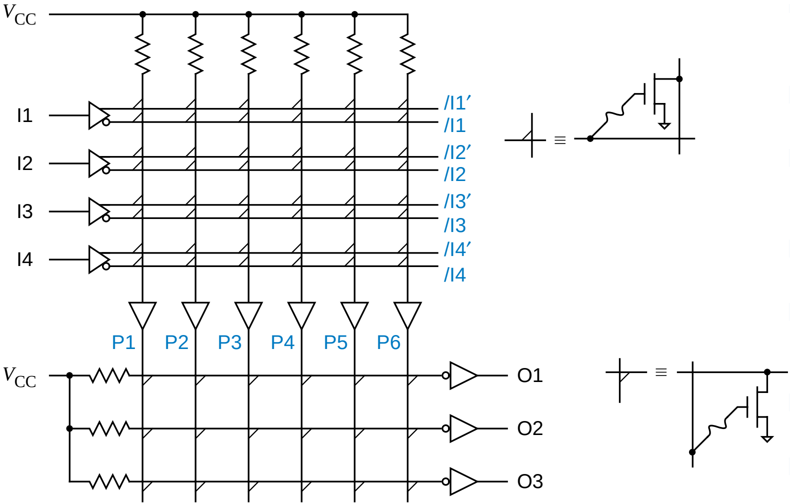

Figure 12: A 4 × 3 PLA built using CMOS logic.

Combinational PLDs: CMOS PLD Circuits

- In Fig. 12
  - An *n*-channel transistor with a programmable connection is placed at each intersection between an input line and a word line
  - If input is LOW, transistor is off, but if input is HIGH, transistor is on, which pulls AND line LOW
  - Overall, an inverted-input AND (NOR) function is obtained
  - Effects of using an inverted-input AND gate are canceled by using complemented input lines for each input
  - Outputs of first-level AND functions are combined by another set of NOR functions with programmable connections
  - Output of each NOR function is followed by an inverter, so an OR function is realized
  - Overall, PLA performs an AND-OR function as desired
  - In CMOS PLD technologies, programmable links are not normally fuses
    - In non-field-programmable devices, such as custom VLSI chips, presence or absence of each link is established as part of metal mask pattern for manufacture of device
    - The most common programming technology is electrical

Combinational PLDs: CMOS PLD Circuits

- **Electrically erasable programmable logic device (EEPLD)**
  - An EEPLD can be programmed with any desired link configuration electrically, as well as erased to its original state
  - EEPLDs use a technology called ”floating-gate MOS”

Combinational PLDs: CMOS PLD Circuits

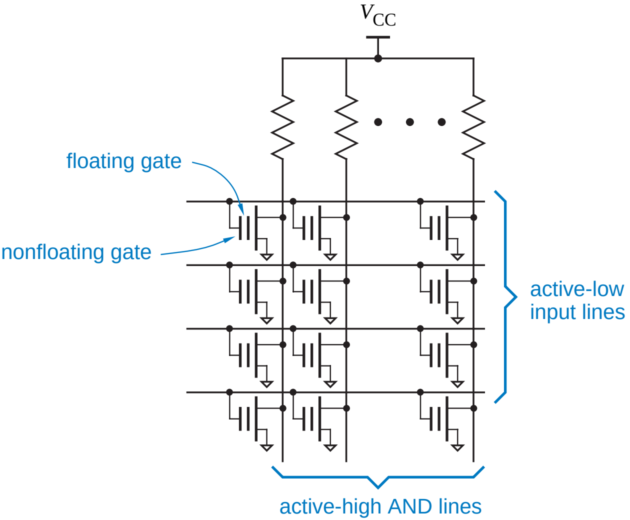

Figure 13: AND plane of an EEPLD using floating-gate MOS transistors.

Combinational PLDs: CMOS PLD Circuits

- A floating-gate MOS transistor has two gates
  - Floating gate is unconnected and is surrounded by extremely high-impedance insulating material
  - In manufactured state, floating gate has no charge on it and has no effect
    - Hence, all transistors are connected
  - To program, we apply a high voltage to non-floating gate at each location where a logical link is not wanted
    - This causes a temporary breakdown in insulating material and allows a negative charge to accumulate on floating gate
    - When high voltage is removed, negative charge remains on floating gate
    - Negative charge prevents transistor from turning "on" when a HIGH signal is applied to nonfloating gate
    - Transistor is disconnected from circuit

Combinational PLDs: CMOS PLD Circuits

- EEPLDs can also be erased
  - Floating gates in an EEPLD are surrounded by an extremely thin insulating layer and can be erased by applying a voltage of opposite polarity as the charging voltage to nonfloating gate
  - The same piece of equipment used to program a PLD can be used to erase an EEPLD before programming it
- Most CPLDs also use floating-gate programming and erasing technology
- FPGAs use read/write memory cells to control state of each connection
  - Read/write memory cells are volatile
  - When power is first applied to FPGA, all of its read/write memory must be initialized to a state specified by a separate, external nonvolatile memory
  - This memory is either a programmable read-only memory (PROM) chip attached to FPGA or is part of a microprocessor subsystem that initializes FPGA as part of overall system initialization

Combinational PLDs: Device Programming and Testing

- A **PLD programmer** or a **PROM programmer** is a special piece of equipment used to vaporize fuses or charge up floating-gate transistors
  - It includes sockets that physically accept devices to be programmed
  - To download desired programming patterns into programmer, it is connected to a PC
- Many PLDs feature **in-system programmability**
  - Device can be programmed after it is soldered into system
  - Fuse patterns are applied to device serially using four extra signals and pins called **JTAG port**, defined by IEEE standard 1149.1
  - These signals are defined so that multiple devices on same printed-circuit board can be "daisy chained" and selected and programmed during board manufacturing process using just one JTAG port on a special connector
  - Fuse patterns are verified as they are programmed into a device
  - Verifying fuse pattern does not prove that device will perform logic function specified by those fuses
    - Device may have unrelated internal defects
    - The only way to test for all defects is to put device into its normal operational mode, apply test-vector inputs, and check outputs against expected results

References

- John F. Wakerly, *Digital Design: Principles and Practices (4th Edition)*, Prentice Hall, 2005.